Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for reducing dark current within an interline CCD image sensor comprising the steps of:

providing the interline CCD image sensor with a matrix of pixels arranged in a plurality of rows and columns with a vertical shift register allocated for each of the columns and at least one horizontal shift register operatively coupled to the vertical shift registers, wherein each of the columns of pixels are formed with the vertical shift registers having a plurality of phases allocated for each of the pixels and a plurality of gate electrodes of the vertical shift register for each of the pixels, and clocking means for causing the transfer of charge from the pixels to the vertical shift registers and through the horizontal shift register;

applying, at a first time period, a first set of voltages to the phases of the gate electrodes of the vertical shift registers sufficient to accumulate holes substantially at a surface of the image sensor in the vertical shift register, beneath each gate electrode;

applying, at a second time period, a second voltage to a first set of the gate electrodes while simultaneously applying a more positive voltage to a second set of gate electrodes, the second voltage being of sufficient potential so holes that were accumulated beneath the second set of gate electrodes during the first time are collected and stored beneath the first set of gate electrodes during the second time period;

applying, at a third time period, a third voltage to the second set of gate electrodes while simultaneously applying a more positive voltage to the first set of gate electrodes, such that the previously accumulated holes beneath the first set of gate electrodes are transferred beneath the second set of gate electrodes; and

returning the first and second sets of gate electrode voltages to their levels at the first time period.

2. (Original) The method of claim 1 further including the step of applying voltages to the first and second sets of gate electrodes between the third

applying step and the returning step to cause excess charge to be returned under the preceding gate electrode.

3. (Original) The method of claim 1 wherein the vertical shift registers are two-phase devices and wherein the third voltage is at substantially the same voltage as the second voltage.

4. (Original) The method of claim 2 wherein the step of applying the first voltage to the phases of the vertical shift registers occurs during a readout period of the horizontal shift register.

5. (Original) The method of claim 1 wherein the image sensor is an interline transfer type image sensor.

6. (Original) The method of claim 1 wherein an additional positive voltage pulse is applied to a first set of gate electrodes during a period of more positive voltage, while simultaneously applying a negative pulse to the second set of gate electrodes.